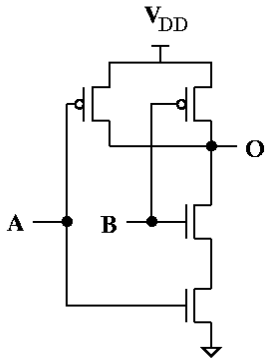
# How Computers Work

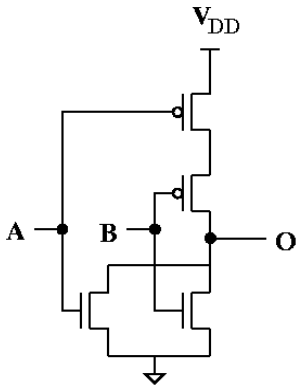
# Problem Set 4

## Problem 1: (Warm-up -- work alone)

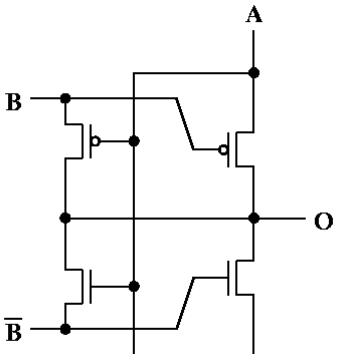
**a**



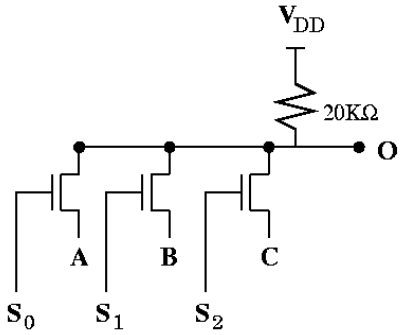

**b**



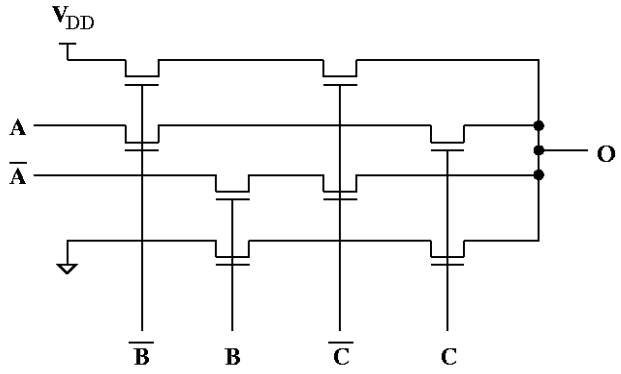

**c**



**d**




**e**



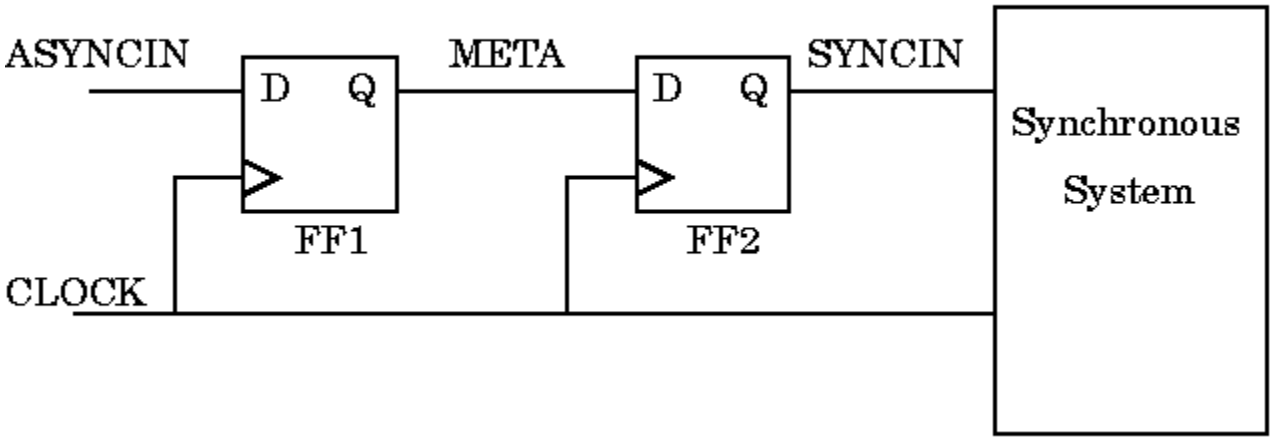

A. For the above circuits , determine the logic function implemented. Wire connections are determined as follows: Anywhere there is a black dot on top of two or more wires, they are electrically connected. If two wires cross and there is no black dot, there is no connection. If three wires intersect in a T, they are connected, whether there is a dot or not. When a wire runs perpendicularly across the gate of a MOS transistor, the wire connects to the gate terminal. For circuit d) assume only one of *S_0, S_1,* or *S_2* can be high at a time.

B. Suppose a datasheet specifies for an inverter: *Vil* = 1.2 V, *Vih* = 3.8 V, with VDD = 5 V. What must the minimum gain of the device be in the forbidden region to ensure noise margins on both ends of at least 0.5V?

# Problem 2: (Collaborative)

The diagram below is supposed to be a synchronizer system which enables one to provide an asynchronous input to a synchronous system by clocking it through two flip-flops. The idea is that even though FF1 may be put into the meta-stable state, the output of FF2 will be valid when required by the synchronous system,

provided the meta-stability in FF1 doesn't last too long. If it does, there is a synchronizer failure.



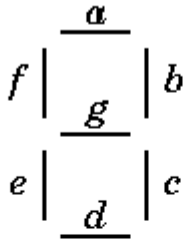

A. Assuming zero contamination delay and zero hold time for the flip-flops, what is the longest duration that a meta-stable state can persist in FF1 without causing failure? Give your answer in terms of the clock period and the setup time of the flip-flops.

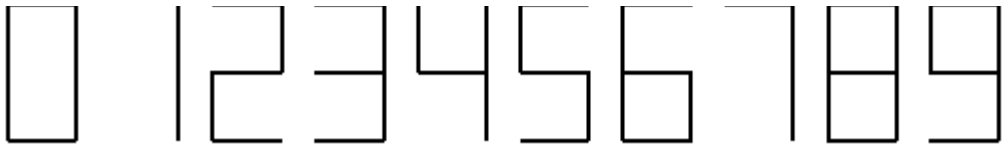
B. Marginal Devices is marketing a system like this one, and Ben Bitdiddle is the chief designer. He has chosen to implement the synchronizer with an old TTL technology flip-flop that has a 20ns setup time. Assume the internal gain of the circuit inside the flip-flops is 10 with a delay time constant, $\tau$ = 2ns. Also, assume the clock period is 100 ns. How long will it take, on average, before the synchronizer fails if the input (ASYNCIN) changes at a 100KHz rate, with roughly a 500ns rise/fall time? If Marginal sells 5000 of these devices per year, how many failures should they expect to deal with in one year?

C. Marginal's synchronizer was so successful that they decide to put out a second version. Ben Bitdiddle has left the company to go get his Ph.D, and Louis Reasoner, recently laid off from Nonlinear Technology, is now the chief designer. Since---as we all know---faster is better, he decides to replace the old system clock with one that runs at 20MHz. In addition, the marketing department launches a successful ad campaign that leads to sales of 10000 units per year. How long should it take for them to get their first complaint from an irate customer?

# Problem 3: (Non-collaborative)

A 7-segment display is often used to display decimal numbers. Shown below is one unit, with the segments labeled *a*-*g*, and the numbers that it should be able to display.





A. Assuming the input is a 4-bit (positive only) number, write the truth table that takes 4 input bits and generates 7 bits of output.

B. Write the Boolean function in sum-of-products form, for each segment, *a*-*g*.

C. Design a PLA, as shown in lecture with a NAND plane and a NOR plane, to implement the 7-segment display.